REMARKS

I. Introduction

In response to the Office Action dated March 13, 2006, Applicants have amended claims 1, 4, 5 and 10-13. Claim 1 was amended in order to clarify the intended subject matter of the invention. Support for the amendment to claim 1 may be found, for example, on page 33, line 17 to page 34, line 5 of the specification. Claims 4, 5 and 10-13 were amended to indicate their status as independent claims. No new matter has been added.

Applicants note with appreciation the indication of allowable subject matter recited by claims 4-7, 10-19 and 21 of the present invention.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claims 1-3, 8-9 And 20 Under 35 U.S.C. § 102

Claims 1-3, 8-9 and 20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Nishizawa et al. (U.S. 2001/0011766). Applicants respectfully submit that Nishizawa fails to anticipate the pending claims for at least the following reasons.

With regard to the present invention, amended claim 1 recites, in-part, a semiconductor device including a plurality of layers of semiconductor chips having substantially the same outer contour, with an integrated circuit being formed on a principal face of each semiconductor chip, the semiconductor chip comprising: a non-conductive layer having a conductive portion provided thereon, and an internal connection member for internally connecting the integrated circuits formed on the plurality of semiconductor chips via the conductive portion provided on the non-conductive layer, an external lead, which is electrically separated from said internal connection member, for connecting the semiconductor device to an external device.

As can be seen in Fig. 8 of the present invention, the connection members 410 and the external connection members 411 all are formed by plating portions of the external leads 406, which themselves are composed of non-conductive pieces, pointed out in the narrow section between connection members 410 and 411. In other words, the connection member 411 is not electrically connected to the internal connection member 410.

In contrast to the present invention, Nishizawa fails to disclose a semiconductor device that has an external lead, which is electrically separated from the internal connection member, for connecting the semiconductor device to an external device. For example, paragraph [0133] of Nishizawa, which states, "the bonding wires can be shortened as a whole compared to the case of connecting the controller chip 33 to the external terminals 52a, 52b..." teaches that the external terminals are connected to internal connection members, the controller chip 33 being an example. In fact, nowhere does the Nishizawa reference teach that the external terminals are electrically separated from a internal connection member. Accordingly, Nishizawa fails to anticipate claim 1 of the present invention.

The significance of this difference is disclosed on pages 35, lines 13-21 of the specification which states,

> "the connection members 410 and the external connection members 411 are formed by plating portions of the external leads 406, which themselves are composed of non-conductive pieces. In other words, the connection members 410 are integral parts of the external leads 406. Therefore, it is unnecessary to employ any additional support member in order to introduce connection members 410. As a result, the number of component elements in the present semiconductor device can be reduced..."

Additionally, page 35, line 22 through page 36, line 2 points out,

> "...positioning of the connection members 410 can be finalized during the positioning of the external leads 406. This makes it unnecessary to pay further attention to the positioning of the connection members 410 during the assembly of the semiconductor device itself."

Thus, the benefit of the above described limitation is to reduce the number of elements in the semiconductor, and to simplify the manufacture of the semiconductor, thereby lowering cost of production. Accordingly, as can be see by the above cited portions of the specification, the newly added limitation to claim 1 has beneficial qualities for the semiconductor of the present invention. In contrast, as Nishizawa fails to disclose the use of an external leads that is electrically separated from the internal connection member, Nishizawa does not teach or disclose the benefits described above.

Anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently in a prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), and Nishizawa et al. does not disclose a semiconductor device including an internal connection member for internally connecting the integrated circuits formed on the plurality of semiconductor chips via the conductive portion provided on the non-conductive layer, and an external leads, which is electrically separated from said internal connection member, for connecting the semiconductor device to an external device. Therefore, as it is apparent from the foregoing that Nishizawa fails to anticipate amended claim 1 or any dependent claims thereon, Applicants respectfully request that the § 102 rejection be traversed.

III. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all pending dependent claims are also in condition for allowance.

IV. Conclusion

Having responded to all open issues set forth in the Office Action, it is respectfully submitted that all claims are in condition for allowance.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 20277 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF/NDM:kap
Facsimile: 202.756.8087
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